9. The method of claim 2, further comprising steps:

(2) sequentially forming a gate insulation material layer and a semiconductor material layer on the substrate subjected to step (1), and processing the semiconductor material layer by a patterning process to form a pattern comprising an active layer, wherein the gate insulation material layer is used for forming a gate insulation layer; and

(3) sequentially forming a second adhesion enhancement layer, a second copper-bearing metal layer and a photoresist layer on the substrate subjected to step (2), and respectively forming a reserved region and a removal region by performing exposure and development on the photoresist layer using a mask plate, wherein the reserved region corresponds to a pattern forming region; simultaneously processing the second adhesion enhancement layer, the second copper-bearing metal layer and the photoresist layer in the removal region by a single wet etching process, to form a second adhesion enhancement intermediate layer corresponding to the second adhesion enhancement layer, a second copper-bearing metal intermediate layer corresponding to the second copper-bearing metal layer, and the photoresist layer on the second copper-bearing metal intermediate layer in the reserved region; and simultaneously processing the second adhesion enhancement intermediate layer, the second copper-bearing metal intermediate layer and the photoresist layer thereon by a dry etching process, then stripping off the photoresist layer, to form a patterned second adhesion enhancement layer and a patterned second copper-bearing metal layer respectively, wherein the second adhesion enhancement layer is a metal layer for enhancing adhesion of the second copper-bearing metal layer to the active layer.

10. The method of claim 9, wherein the patterned second copper-bearing metal layer is a pattern comprising source electrodes and drain electrodes.

11. The method of claim 10, wherein the pattern comprising source electrodes and drain electrodes comprises source electrodes, drain electrodes and data lines formed in the same layer.

12. The method of claim 9, wherein the material of the second copper-bearing metal layer is copper or copper alloy.

13. The method of claim 9, wherein the material of the second adhesion enhancement layer is any one of tungsten, tantalum, titanium, molybdenum, molybdenum alloy and titanium alloy.

14. The method of claim 9, wherein the thickness of the second adhesion enhancement layer is 100~1000 Å, and the thickness of the second copper-bearing metal layer is 1500~5000 Å.

15. The method of claim 9, wherein after the single wet etching process, the width of the formed second adhesion enhancement intermediate layer is larger than the width of the formed second copper-bearing metal intermediate layer, so that the second adhesion enhancement intermediate layer forms a step structure with respect to the second copper-bearing metal intermediate layer, and the step structure will be removed by a subsequent dry etching process.

16. The method of claim 9, wherein the gate insulation material layer is a mono-layer, double-layer or multi-layer structure composed of oxide, nitride or nitrogen oxide.

17. The method of claim 9, further comprising steps:

(4) forming a passivation layer on the substrate subjected to step (3), and forming a passivation layer pattern comprising via-holes by a patterning process; and

(5) forming a transparent conductive layer on the substrate subjected to step (4), and forming a pattern comprising pixel electrodes by a patterning process, wherein the pixel electrodes are connected with the drain electrodes through the via-holes.

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